

REMARKS

The above application has been amended and reconsideration and re-examination are requested.

In the initialed copy of Form PTO-1449, Examiner indicates errors in Applicants' information disclosure statement. In response, Applicants have filed a supplemental information disclosure statement to correct the errors.

The Examiner rejected claims 1-25 under 35 U.S.C., second paragraph, as being indefinite.

With respect to item 4(a) of Examiner's office action, the multiple contexts of claim 1 are threads of a computer program, as described in page 3 of Applicants' specification. As generally defined, threads are used to execute actions of a computer program. Thus, the definition of "multiple contexts" indicates how they are used.

With respect to item 4(b), Applicants' specification on pages 10 to 11 clearly describes a pipeline comprises pipeline stages that perform functions on data over time intervals. Pipelines and pipeline stages are well-known to those of skill in the art.

With respect to item 4(c), claim 1 has been amended to clarify that the system functions are assigned to the plurality of programming engines.

With respect to item 4(d), claim 2 has been amended to clarify that the tasks performed by the programming engines are synchronized.

With respect to item 4(e) directed to claims 16 and 23, the use of the multiple contexts and the stages of the pipeline have been addressed above with respect to items 4(a-b). Furthermore, assigning functions to corresponding engines is consistent with the concept of a functional pipeline because the functions can be distributed across one or more functional pipelined stages executed by the engines.

With respect to item 4(f), claim 17 has been amended to recite "synchronizing system functions from a first programming engine of the functional pipeline unit to a second programming engine of the functional pipeline unit." Claim 24 has been amended similarly to claim 17.

The Examiner rejected claims 1, 3, 5-9, 16, 19, 20, 23, and 25 under 35 U.S.C. 102(b) as being anticipated by Georgiou et al, U.S. Patent Application 2003/0067913.

Claim 1 has been amended to include "a critical section that provides exclusive privileges to one of the multiple contexts for modifying a shared resource." As described in Applicants' specification on pages 13 to 14, the critical section represents code which provides exclusive privileges to a programming engine context for modifying a shared resource. As seen in Applicants' FIG. 5, the critical section (e.g., critical section 82a) controls access to shared data (e.g., critical data 86a). Furthermore, as described on page 14 of Applicants' specification, only one programming engine transitions to a critical section at any given time to ensure that shared data is not modified simultaneously by two or more programming engines.

Georgiou neither describes nor suggests a critical section that provides exclusive privileges to one of the multiple contexts for modifying a shared resource as recited in claim 1. In FIG. 1, Georgiou discloses processors 107 through 110 having access to a shared external memory over a high-speed interconnect 111; however, Georgiou does not disclose a critical section that provides exclusive privileges to one of the processors for modifying the shared external memory.

In FIG. 2 and accompanying text in par. 24, Georgiou discloses local memory 202 of a processor being shared between threads of the processor and threads of other processors. The processor shown in FIG. 2, however, does not have a critical section that provides exclusive privileges to one of the thread units for modifying the shared local memory 202.

In FIG. 3 and accompanying text in par. 29 to par. 30, Georgiou discloses several identical processor threads (e.g., threads 304 through 305) connected to a shared memory 300 over a high-speed interconnect 201. FIG. 3 and accompanying text in par. 29 to par. 30, however, do not teach a critical section. Rather, Georgiou in par. 53 discloses a master thread that provides pointers to available memory blocks to each of the threads 304 through 305. Georgiou, however, neither discloses nor suggests the master thread 303 providing exclusive privileges to one of the threads 304 through 305 for modifying the shared memory 300.

In par. 9, Georgiou describes a front-end hardwired logic for handling time critical operations; however, the front-end hardwired logic is neither described nor suggested to provide exclusive privileges to one of multiple contexts for modifying a shared resource. Rather, the front-end hardwired logic pre-processes incoming data at the network interface (e.g., by encoding/decoding packets, checking data for errors, reading header bits, etc.) before transmitting the data to the processors. Applicants' critical section, on the other hand, interacts with a processor at various functional pipeline stages during the execution of a thread.

For at least the foregoing reasons, claim 1 is patentable over the reference. The limitations of claims 16 and 23 are similar to the limitations of claim 1 and thus claims 16 and 23 are patentable. Applicants' dependent claims are allowable at least for the reasons discussed above and also define patentable features over the art.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claims, except as specifically stated in this paper, and the amendment of any claims does not necessarily signify concession of unpatentability of the claim prior to its amendment. The prior art cited but not applied by the Examiner is seen as neither describing nor suggesting Applicants' invention whether taken separately or in combination with the art applied.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested.

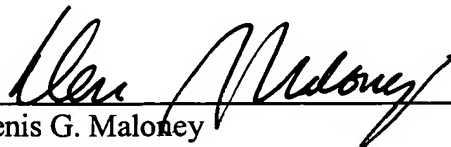
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Respectfully submitted,

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